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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,447	10/26/2001	Timothy J. Dalton	FIS920010239US1	3611
7590	02/26/2004		EXAMINER	
Sean F. Sullivan, Esq. Cantor Colburn LLP 55 Griffin Road South Bloomfield, CT 06002			LEWIS, MONICA	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/002,447

Applicant(s)

DALTON ET AL.

Examiner

Monica Lewis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 10-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

1. This action is in response to the request for continued examination filed October 10, 2003.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/10/03 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Srikrishnan et al. (U.S. Patent No. 5,389,814).

In regards to claim 1, Srikrishnan et al. ("Srikrishnan") discloses the following:

a) a conductive layer (400), said conductive layer completing a conductive path between wiring segments included a wiring layer (For Example: See Figure 4e);

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b) an organic material (350) encapsulated underneath said conductive layer (For Example: See Figure 4e); and

c) the fuse structure is blown open by application of a beam of laser energy thereto (For Example: See Column 1 Lines 48-50).

In regards to claim 3, Srikrishnan discloses the following:

a) organic material is selected from a group that includes a polyimide, a polyamide, a polyarylene ether, a polyaromatic hydrocarbon (PAH), and a conductive polyaniline (For Example: Column 6 Lines 56 and 57).

6. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwala et al. (U.S. Patent No. 6,033,939).

In regards to claim 1, Agarwala et al. ("Agarwala") discloses the following:

a) a conductive layer (10), said conductive layer completing a conductive path between wiring segments included a wiring layer (For Example: See Figure 4);

b) an organic material (8) encapsulated underneath said conductive layer (For Example: See Figure 4); and

c) the fuse structure is blown open by application of a beam of laser energy thereto (For Example: See Column 1 Lines 23 and 24).

In regards to claim 3, Agarwala discloses the following:

a) organic material is selected from a group that includes a polyimide, a polyamide, a polyarylene ether, a polyaromatic hydrocarbon (PAH), and a conductive polyaniline (For Example: Column 7 Lines 5-23).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as obvious over Srikrishnan et al. (U.S. Patent No. 5,389,814) in view of Stamper (U.S. Patent No. 6,111,301).

In regards to claims 2 and 4, Srikrishnan fails to disclose the following:

a) a liner material selected from a group that includes TaN, Ta, TiN, Ti, W, WN, TaSiN, TiSiN, or alloys therefrom in electrical contact with said wiring segments and said conductive layer, said liner material further encapsulating said organic material between said wiring layer and said conductive layer.

However, Stamper discloses the use of liners (For Example: See Column 2 Lines 45-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Srikrishnan to include the use of liners as disclosed in Stamper because it is resistant to corrosion and aids in separating the wiring (For Example: See Column 2 Lines 45-65).

Additionally, since Srikrishnan and Stamper are both from the same field of endeavor, the purpose disclosed by Stamper would have been recognized in the pertinent art of Srikrishnan.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as obvious over Srikrishnan et al. (U.S. Patent No. 5,389,814) in view of Lee et al. (U.S. Patent No. 6,300,233).

In regards to claim 5, Srikrishnan fails to disclose the following:

a) conductive layer is selected from a group that includes TaN, Ta, TiN, Ti, W, WN, TaSiN, TiSiN, or alloys therefrom.

However, Lee discloses the use of TiN and W (For Example: See Column 3 Lines 43 and 44 and Column 4 Lines 33-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Srikrishnan to include the use TiN or W as disclosed in Lee because it provides dense physical properties (For Example: See Column 4 Lines 53-56).

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Additionally, since Srikrishnan and Lee are both from the same field of endeavor, the purpose disclosed by Lee would have been recognized in the pertinent art of Srikrishnan.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as obvious over Srikrishnan et al. (U.S. Patent No. 5,389,814) in view of Stamper (U.S. Patent No. 6,111,301) and Agarwala et al. (U.S. Patent No. 6,033,939).

In regards to claim 6, Srikrishnan fails to disclose the following:

a) a pair of vias formed within an insulating layer and extending down to said wiring segments; and a mesa region of said insulating layer formed between said pair of vias.

However, Agarwala discloses the vias (9) formed within an insulating layer (6) and extending down to said wiring segments and a mesa region of said insulating layer formed between said pair of vias (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Srikrishnan to include vias formed within an insulating layer and extending down to said wiring segments and a mesa region of said insulating layer formed between said pair of vias as disclosed in Agarwala because it aids in providing high density (For Example: See Column 1 Lines 48 and 49).

Additionally, since Srikrishnan and Agarwala are both from the same field of endeavor, the purpose disclosed by Agarwala would have been recognized in the pertinent art of Srikrishnan.

b) liner material is formed upon sides of said mesa region and said wiring segments.

However, Stamper discloses the use of liners (For Example: See Column 2 Lines 45-65). It would have been obvious to one having ordinary skill in the art at the time the invention was

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made to modify the semiconductor device of Srikrishnan to include the use of liners as disclosed in Stamper because it is resistant to corrosion and aids in separating the wiring (For Example: See Column 2 Lines 45-65).

Additionally, since Srikrishnan and Stamper are both from the same field of endeavor, the purpose disclosed by Stamper would have been recognized in the pertinent art of Srikrishnan.

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as obvious over Srikrishnan et al. (U.S. Patent No. 5,389,814) in view of Stamper (U.S. Patent No. 6,111,301), Agarwala et al. (U.S. Patent No. 6,033,939) and DiStefano et al. (U.S. Patent No. 5,590,460).

In regards to claim 7, Srikrishnan fails to disclose the following:

a) pair of vias is filled with said organic material.

However, DiStefano et al. ("DiStefano") discloses the use of organic material in vias (For Example: See Column 13 Lines 4-13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Srikrishnan to include the use of organic material as disclosed in DiStefano because it remains solid at temperatures below the activation temperature (For Example: See Column 13 Lines 4-13).

Additionally, since Srikrishnan and DiStefano are both from the same field of endeavor, the purpose disclosed by DiStefano would have been recognized in the pertinent art of Srikrishnan.

In regards to claim 8, Srikrishnan discloses the following:

a) organic material further occupies an inner area of the fuse structure (For Example: See Figure 4e).

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In regards to claim 8, Srikrishnan fails to disclose the following:

a) organic material occupies the inner area between the top of said mesa region and said conductive layer.

However, Agarwala discloses organic material that occupies the inner area between the top of said mesa region and said conductive layer (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Srikrishnan to include organic material that occupies the inner area between the top of said mesa region and said conductive layer as disclosed in Agarwala because it aids in providing high resistance (For Example: See Column 7 Lines 5-18).

Additionally, since Srikrishnan and Agarwala are both from the same field of endeavor, the purpose disclosed by Agarwala would have been recognized in the pertinent art of Srikrishnan.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as obvious over Srikrishnan et al. (U.S. Patent No. 5,389,814) in view of Stamper (U.S. Patent No. 6,111,301), Agarwala et al. (U.S. Patent No. 6,033,939), DiStefano et al. (U.S. Patent No. 5,590,460) and *Electronic Packaging and Interconnection Handbook* by Charles A. Harper.

In regards to claim 9, Srikrishnan fails to disclose the following:

a) conductive layer covers said inner area and organic material, thereby completing said conductive path.

Although Agarwala does not specifically state that (10) is a conductive layer and a top view of Figure 4 is not shown, it is well known in the art to use conductive layers with solder balls and conductive lines as shown in Harper (For Example: See Figure 10.35). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

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made to modify the semiconductor device of Srikrishnan to include the metal traces as disclosed in Harper because they aid in establishing electrical communication (For Example: See Figure 10.35).

Additionally, since Srikrishnan, Agarwala and Harper are both from the same field of endeavor, the purpose disclosed by Agarwala and Harper would have been recognized in the pertinent art of Srikrishnan.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as obvious over Agarwala et al. (U.S. Patent No. 6,033,939) in view of DiStefano et al. (U.S. Patent No. 5,590,460).

In regards to claim 18, Agarwala discloses the following:

a) an electrically conductive organic material (5), said electrically conductive material completing a conductive path between wiring segments included in a wiring layer (For Example: Figure 4);

b) a pair of vias (9) formed within an insulating layer (6), said pair of vias extending down to said wiring segments (For Example: See Figure 4); and

c) the fuse structure is blown open by application of a beam of laser energy to said electrically conductive material (For Example: See Column 1 Lines 23 and 24).

In regards to claim 18, Agarwala fails to disclose the following:

a) an organic material filling the vias.

However, DiStefano discloses the use of organic material in vias (For Example: See Column 13 Lines 4-13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use of organic material as disclosed in DiStefano because it remains solid at temperatures below the activation temperature (For Example: See Column 13 Lines 4-13).

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Additionally, since Agarwala and DiStefano are both from the same field of endeavor, the purpose disclosed by DiStefano would have been recognized in the pertinent art of Agarwala.

14. Claims 2, 4 and 6 are rejected under 35 U.S.C. 103(a) as obvious over Agarwala et al. (U.S. Patent No. 6,033,939) in view of Stamper (U.S. Patent No. 6,111,301).

In regards to claim 2, Agarwala fails to disclose the following:

a) a liner material in electrical contact with said wiring segments and said conductive layer, said liner material further encapsulating said organic material between said wiring layer and said conductive layer.

However, Stamper discloses the use of liners (For Example: See Column 2 Lines 45-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use of liners as disclosed in Stamper because it is resistant to corrosion and aids in separating the wiring (For Example: See Column 2 Lines 45-65).

Additionally, since Agarwala and Stamper are both from the same field of endeavor, the purpose disclosed by Stamper would have been recognized in the pertinent art of Agarwala.

In regards to claim 4, Agarwala fails to disclose the following:

a) liner material is selected from a group that includes TaN, Ta, TiN, Ti, W, WN, TaSiN, TiSiN, or alloys therefrom.

However, Stamper discloses the use of liners (For Example: See Column 2 Lines 45-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use of liners as disclosed in Stamper because it is resistant to corrosion and aids in separating the wiring (For Example: See Column 2 Lines 45-65).

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Additionally, since Agarwala and Stamper are both from the same field of endeavor, the purpose disclosed by Stamper would have been recognized in the pertinent art of Agarwala.

In regards to claim 6, Agarwala discloses the following:

a) a pair of vias (9) formed within an insulating layer (6) and extending down to said wiring segments (For Example: See Figure 4); and

b) a mesa region of said insulating layer formed between said pair of vias (For Example: See Figure 4).

In regards to claim 6, Agarwala fails to disclose the following:

a) liner material is formed upon sides of said mesa region and said wiring segments.

However, Stamper discloses the use of liners (For Example: See Column 2 Lines 45-65). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use of liners as disclosed in Stamper because it is resistant to corrosion and aids in separating the wiring (For Example: See Column 2 Lines 45-65).

Additionally, since Agarwala and Stamper are both from the same field of endeavor, the purpose disclosed by Stamper would have been recognized in the pertinent art of Agarwala.

15. Claim 5 is rejected under 35 U.S.C. 103(a) as obvious over Agarwala et al. (U.S. Patent No. 6,033,939) in view of Lee et al. (U.S. Patent No. 6,300,233).

In regards to claim 5, Agarwala fails to disclose the following:

a) conductive layer is selected from a group that includes TaN, Ta, TiN, Ti, W, WN, TaSiN, TiSiN, or alloys therefrom.

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However, Lee discloses the use of TiN and W (For Example: See Column 3 Lines 43 and 44 and Column 4 Lines 33-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use TiN or W as disclosed in Lee because it provides dense physical properties (For Example: See Column 4 Lines 53-56).

Additionally, since Agarwala and Lee are both from the same field of endeavor, the purpose disclosed by Lee would have been recognized in the pertinent art of Agarwala.

16. Claims 7-9 are rejected under 35 U.S.C. 103(a) as obvious over Agarwala et al. (U.S. Patent No. 6,033,939) in view of Stamper (U.S. Patent No. 6,111,301) and DiStefano et al. (U.S. Patent No. 5,590,460).

In regards to claim 7, Agarwala fails to disclose the following:

a) pair of vias is filled with said organic material.

However, DiStefano discloses the use of organic material in vias (For Example: See Column 13 Lines 4-13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Agarwala to include the use of organic material as disclosed in DiStefano because it remains solid at temperatures below the activation temperature (For Example: See Column 13 Lines 4-13).

Additionally, since Agarwala and DiStefano are both from the same field of endeavor, the purpose disclosed by DiStefano would have been recognized in the pertinent art of Agarwala.

In regards to claim 8, Agarwala discloses the following:

a) organic material further occupies an inner area of the fuse structure, said inner area between the top of said mesa region and said conductive layer (For Example: See Figure 4).

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In regards to claim 9, Agarwala discloses the following:

a) conductive layer covers said inner area and organic material, thereby completing said conductive path (For Example: See Figure 4 and Column 7 Lines 5-23).

Conclusion

17. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Kawanishi (U.S. Patent No. 5,982,268) discloses a thin fuse.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
February 5, 2004



**Mary Wilczewski
Primary Examiner**